AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [005] with the following amended paragraph:

[005] In the past, measuring a propagation delay through a device and/or cables used to connect these devices was a costly operation. For example, an ~~Agilent®~~ AGILENT®-brand Digital Communication Analyzer (Serial BERT 3.6 Gb/s Bit Error Ration Testor) which currently retails for more than nincty thousand dollars was required to take such measurements with precision comparable to that of the present invention.

Please replace paragraph [021] with the following amended paragraph:

[021] The Scrializer/Deserializer (SERDES) 20 can be a device for receiving data in parallel and transmitting this data serially. One example of such a device would be an ~~ON Semiconductor@~~ ON SEMICONDUCTOR®-brand 8-Bit parallel to serial converter MC1O0EP446. As illustrated in Figure 1, SERDES 20 includes a D_{in} port 22 and a D_{out} port 24. The D_{in} port 22 can receive bit groups in parallel and D_{out} port 24 can serially transmit bit groups received through D_{in} port 22.

Please replace paragraph [023] with the following amended paragraph:

[023] The programmable delay 30 includes a D_{in} port 32, a D_{out} port 34, and an I/O port 36. The programmable delay 30 can be a programmable delay circuit, such as an ~~ON Semiconductor@~~ ON SEMICONDUCTOR®-brand ECL Programmable Delay Chip MC1O0EPI96. A data signal applied to an input 32 of programmable delay 30 reappears at an output 34 of programmable delay 30, after a delay of a specified amount of time. Both leading and trailing edges of data signal pulses are delayed by the same amount of time, which is typically programmable by controller 120 using either a serial or parallel data input.

Please replace paragraph [025] with the following amended paragraph:

[025] The deserializer 90 can be a device, such as a MICREL 3.3V ~~AnyRate~~ ANYRATE®-brand MUX/DEMUX SY87724L, for receiving data serially and transmitting this data in parallel. As illustrated in Figure 1, deserializer 90 includes a D_{in} port 92 and a D_{out} port 94. The D_{in} port 92 receives bit groups serially and D_{out} port 94 transmits these bit groups in parallel. The deserializer 90 can also include one or more ports (not illustrated) for exchanging control signals with controller 120. These ports enable controller 120 to, for example, control how deserializer 90 receives, transforms, and transmits data.

Please replace paragraph [026] with the following amended paragraph:

[026] The controller 120 includes a computer processor on a microchip such as a ~~Motorola®~~ MOTOROLA®-brand bit processor or other chip combining an 8-bit architecture with an array of field-programmable logic. The controller 120 directs the operation of circuitry on circuit board 2 (not all connections illustrated) and stores and manipulates data provided by this circuitry. Controller 120 completes these tasks, under the direction of computer 160. In some embodiments of the present invention, controller 120 may not have the capacity to perform measurements, which are described below, without computer 160.

Please replace paragraph [032] with the following amended paragraph:

[032] The clock source 150 is designed to provide a clock signal at a desired frequency. The clock source 150 can be a single, self contained circuit such as an ~~Amptron®~~ AMPTRON®-brand or ~~Cardinal Components, Inc.~~ CARDINAL COMPONENTS, INC.®-brand crystal based oscillator. Such circuits are single frequency circuits, but clock source 150 can also have multiple-frequency capability. The clock source 150 can also have a plurality of circuits including a primary circuit and external timing components. In an exemplary embodiment, clock

source 150 is capable of generating a clock signal at a frequency on the order of one picosecond or less.